IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

Claims 1-6 (canceled)

7. (new) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate ; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided exclusively on said another side of said substrate.

8. (new) A semiconductor multi-chip module according to claim 7, wherein said substrate is a multilayer wiring substrate.

9. (new) A semiconductor multi-chip module according to claim 8, wherein said multilayer wiring substrate is a ceramic substrate.

10. (new) A semiconductor multi-chip module according to claim 7, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

11. (new) A semiconductor multi-chip module according to claim 7, wherein a checking function is provided for detecting faults in said semiconductor chips.

12. (new) A semiconductor multi-chip module according to claim 11, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

13. (new) A semiconductor multi-chip module according to claim 7, wherein at least one of said semiconductor chips is a memory for storing data.

14. (new) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided exclusively on said another side of said substrate,

wherein said first data lines correspond to a portion of a plurality of bits of a data signal formed by a portion of said data lines and said second data lines correspond to another portion of the bits of the data signal formed by another portion of said data lines.

15. (new) A semiconductor multi-chip module according to claim 14, wherein said substrate is a multilayer wiring substrate.

16. (new) A semiconductor multi-chip module according to claim 15, wherein said multilayer wiring substrate is a ceramic substrate.

17. (new) A semiconductor multi-chip module according to claim 14, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

18. (new) A semiconductor multi-chip module according to claim 14, wherein a checking function is provided for detecting faults in said semiconductor chips.

19. (new) A semiconductor multi-chip module according to claim 18, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor when faults of said processor are detected.

20. (new) A semiconductor multi-chip module according to claim 14, wherein at least one of said semiconductor chips is a memory for storing data.

21. (new) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided exclusively on said another side of said substrate,

wherein said first data lines corresponding to upper bits of said data lines and said second data lines corresponding to lower bits of said data lines.

22. (new) A semiconductor multi-chip module according to claim 21, wherein said substrate is a multilayer wiring substrate.

23. (new) A semiconductor multi-chip module according to claim 22, wherein said multilayer wiring substrate is a ceramic substrate.

24. (new) A semiconductor multi-chip module according to claim 21, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

25. (new) A semiconductor multi-chip module according to claim 21, wherein a checking function is provided for detecting faults in said semiconductor chips.

26. (new) A semiconductor multi-chip module according to claim 25, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said when faults of said processor are detected.

27. (new) A semiconductor multi-chip module according to claim 21, wherein at least one of said semiconductor chips is a memory for storing data.

28. (new) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate ; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate.

29. (new) A semiconductor multi-chip module according to claim 28, wherein said substrate is a multilayer wiring substrate.

30. (new) A semiconductor multi-chip module according to claim 29, wherein said multilayer wiring substrate is a ceramic substrate.

31. (new) A semiconductor multi-chip module according to claim 28, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

32. (new) A semiconductor multi-chip module according to claim 28, wherein a checking function is provided for detecting faults in said semiconductor chips.

33. (new) A semiconductor multi-chip module according to claim 32, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

34. (new) A semiconductor multi-chip module according to claim 28, wherein at least one of said semiconductor chips is a memory for storing data.

35. (new) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate,

wherein said first data lines correspond to a portion of a plurality of bits of a data signal formed by a portion of said data lines and said second data lines correspond to another portion of the bits of the data signal formed by another portion of said data lines.

36. (new) A semiconductor multi-chip module according to claim 35, wherein said substrate is a multilayer wiring substrate.

37. (new) A semiconductor multi-chip module according to claim 36, wherein said multilayer wiring substrate is a ceramic substrate.

38. (new) A semiconductor multi-chip module according to claim 35, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

39. (new) A semiconductor multi-chip module according to claim 35, wherein a checking function is provided for detecting faults in said semiconductor chips.

40. (new) A semiconductor multi-chip module according to claim 39, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

41. (new) A semiconductor multi-chip module according to claim 35, wherein at least one of said semiconductor chips is a memory for storing data.

42. (new) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate,

wherein said first data lines corresponding to upper bits of said data lines and said second data lines corresponding to lower bits of said data lines.

43. (new) A semiconductor multi-chip module according to claim 42, wherein said substrate is a multilayer wiring substrate.

44. (new) A semiconductor multi-chip module according to claim 43, wherein said multilayer wiring substrate is a ceramic substrate.

45. (new) A semiconductor multi-chip module according to claim 42, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

46. (new) A semiconductor multi-chip module according to claim 42, wherein a checking function is provided for detecting faults in said semiconductor chips.

47. (new) A semiconductor multi-chip module according to claim 46, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said when faults of said processor are detected.

48. (new) A semiconductor multi-chip module according to claim 42, wherein at least one of said semiconductor chips is a memory for storing data.